REMARKS

These remarks will respond to the rejections of the office action of June 2, 2004.

A. Status of Claims:

Claims 31-40 are pending in the application. Claims 36 and 39-40 were rejected under 35 USC 112. Claims 31-38 were rejected under 35 USC 102(e) as being anticipated by Knall et al., US Patent No. 6,420,215.

B. Claims 36 and 39-40, 112 rejection

Claims 36 and 39-40 were rejected under 35 USC 112, second paragraph.

Regarding claim 36, the Examiner says:

> ... it is unclear how the first second and third rail-stacks have approximately the same height when the second rail-stack having more layers that that of the first and the third railstacks?

Claim 36 has been amended to recite the process defined by claim 31, wherein the thickness of layers etched in the second and third etch steps is approximately the same.

Regarding claim 39, the Examiner asserts:

> In claim 39, last five lines are confusing and indefinite, since it is unclear as to how could the third rail-stack is (sic) formed by etching the third conductive layer, and the etched fourth semiconductor layer which is covered by the antifuse layer, without etching the antifuse layer?

Applicant believes the Examiner is referring to this portion of the claim:

> ... in a third etch step, etching the third semiconductor layer and third conductive layer to form third parallel, spaced-apart rail-stacks;

This limitation in the claim specifies that the third etch etches the third semiconductor layer and the third conductive layer. Applicant respectfully points out that in specifying layers that are included in the etch, the claim does not explicitly exclude any other layer, such as the antifuse layer, from being etched by the same etch, and such is not properly assumed. It is the

purpose of the specification to provide explicit instructions for making the invention, not of the claims. Thus Applicant respectfully asserts that etching of the antifuse layer need not be included in the claim, and its omission does not render the claim indefinite.

C. Claims 31-38, 102 rejection

Claim 31 was amended to recite a process for fabricating two memory levels in a memory array comprising:

forming a first conductive layer;

depositing a first semiconductor layer over the first conductive layer, the first semiconductive layer being doped with a first conductivity type dopant;

forming a first antifuse layer over the first semiconductor layer;

depositing a second semiconductor layer doped with a second conductivity type dopant over the first antifuse layer;

in a first etch step, etching the first conductive layer, the first semiconductor layer, the first antifuse layer, and the second semiconductor layer into a plurality of first parallel, spaced-apart rail-stacks;

filling the space between the first rail-stacks with a first insulator;

planarizing the first upper surface of the first rail-stacks and the first insulator;

forming a second conductive layer over the second semiconductor layer;

depositing a third semiconductor layer doped with a second conductivity type dopant over the second conductive layer;

in a second etch step, etching the second conductive layer and the third semiconductor layer into a plurality of second parallel, spaced-apart rail-stacks;

filling the space between the second rail-stacks with a second insulator;

planarizing the second upper surface of the second insulator and the second rail-stacks;

forming a second antifuse layer on the planarized second upper surface;

depositing a fourth semiconductor layer doped with a first conductivity type dopant over the second antifuse layer;

forming a third conductive layer;

in a third etch step, etching the third semiconductor layer and third conductive layer to form third parallel, spaced-apart rail-stacks;

filling the space between the third rail-stacks with a third insulator.

As amended, in this claim, the first etch step etches the first conductive layer, the first semiconductor layer, the first antifuse layer, and the second semiconductor layer into a plurality of first parallel, spaced-apart rail-stacks. In Knall, conductive layer 14, semiconductor layer 15, antifuse layer 20 and second semiconductor layer 21 are not etched in the same etch step.

Thus claim 31 and its dependent claims distinguish over the structure of Knall et al. Applicant respectfully requests reconsideration.

CONCLUSION

In view of these amendments and remarks, Applicant submits that this application is in condition for allowance. Reconsideration is respectfully requested. **If any objections or rejections remain, Applicant respectfully requests an interview to discuss the references.** If the Examiner has any questions, he is asked to contact the undersigned agent at (408) 869-2921.

October 1, 2004

Date

Pamela J. Squyres
Agent for Applicant
Reg. No. 52246

Matrix Semiconductor
3230 Scott Blvd
Santa Clara, CA 95054
Tel. 408-869-2921